

Reply to Final Office Action of December 19, 2005  
Amendment Dated: February 6, 2006

Appl. No.: 10/708,800  
Attorney Docket No.: H0005591

Listing of Claims

1 Claim 1 (Canceled)

1 Claim 2 (Currently Amended): A high resolution potentiometer comprising:  
2 a first digital potentiometer and a second digital potentiometer connected in parallel,  
3 wherein said first digital potentiometer is operable to be set to offer a first resistance and said  
4 second digital potentiometer is operable to be set to offer a second resistance, wherein said  
5 first resistance is not equal to said second resistance; and  
a controller block to cause said first digital potentiometer and said second digital  
potentiometer to respectively offer said first resistance and said second resistance.

1 Claim 3 (Canceled)

1 Claim 4 (Currently Amended): The high resolution potentiometer of claim 2 3,  
2 wherein said controller block receives a desired resistance value and sets said first digital  
3 potentiometer to provide said first resistance and said second digital potentiometer to provide  
4 said second resistance such that the effective resistance provided by said high resolution  
5 potentiometer at least substantially equals said desired resistance.

1 Claim 5 (Currently Amended): The high resolution potentiometer of claim 2 3,  
2 wherein said controller block receives values corresponding to said first resistance and said  
3 second resistance, and sets said first digital potentiometer to provide said first resistance and  
4 said second digital potentiometer to provide said second resistance such that the effective  
5 resistance provided by said high resolution potentiometer at least substantially equals a  
6 desired resistance.

1 Claim 6 (Currently Amended): The high resolution potentiometer of claim 2 3, further  
2 comprising a resistor connected in series with said first digital potentiometer and said second  
3 digital potentiometer connected in parallel.

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1       Claim 7 (Previously Amended): A high resolution potentiometer comprising:  
2            a first digital potentiometer and a second digital potentiometer connected in parallel,  
3        wherein said first digital potentiometer is operable to be set to offer a first resistance and said  
4        second digital potentiometer is operable to be set to offer a second resistance, wherein said  
5        first resistance is not equal to said second resistance; and

6            a controller block to cause said first digital potentiometer and said second digital  
7        potentiometer to respectively offer said first resistance and said second resistance.

8            wherein said first potentiometer, said second potentiometer and said controller block  
9        are implemented in a single integrated circuit.

1       Claim 8 (Currently Amended): A system comprising:

2            a first digital potentiometer and a second digital potentiometer connected in parallel,  
3        wherein said first digital potentiometer is operable to be set to offer a first resistance and said  
4        second digital potentiometer is operable to be set to offer a second resistance, wherein said  
5        first resistance is not equal to said second resistance; and

6            a controller block to cause said first digital potentiometer and said second digital  
7            potentiometer to respectively offer said first resistance and said second resistance.

1       Claim 9 (Canceled):

1       Claim 10 (Currently Amended): The system of claim 8 9, wherein said controller  
2       block receives a desired resistance value from said a processor and sets said first digital  
3       potentiometer to provide said first resistance and said second digital potentiometer to provide  
4       said second resistance such that the effective resistance provided by said system at least  
5       substantially equals said desired resistance.

1       Claim 11 (Currently Amended): The system of claim 8 9, wherein said controller  
2       block receives values corresponding to said first resistance and said second resistance from  
3       said a processor, and sets said first digital potentiometer to provide said first resistance and  
4       said second digital potentiometer to provide said second resistance such that the effective

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5 resistance provided by said first digital potentiometer and said second digital potentiometer  
6 are connected in parallel at least substantially equals a desired resistance.

1       Claim 12 (Currently Amended): The system of claim 8 9, further comprising a resistor  
2 connected in series with said first digital potentiometer and said second digital potentiometer  
3 connected in parallel.

1       Claim 13 (Previously Amended): A system comprising:

2           a first digital potentiometer and a second digital potentiometer connected in parallel,  
3 wherein said first digital potentiometer is operable to be set to offer a first resistance and said  
4 second digital potentiometer is operable to be set to offer a second resistance, whereinsaid  
5 first resistance is not equal to said second resistance;

6           a controller block to cause said first digital potentiometer and said second digital  
7 potentiometer to respectively offer said first resistance and said second resistance; and

8           wherein said first potentiometer, said second potentiometer and said controller block  
9 are implemented in the form of a single integrated circuit.

1       Claim 14 (Original): The system of claim 13, further comprising a processor, wherein  
2 said controller block receives a desired resistance value from said processor and sets said  
3 first digital potentiometer to provide said first resistance and said second digital  
4 potentiometer to provide said second resistance such that the effective resistance provided  
5 by said system at least substantially equals said desired resistance.